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65913 7590 10/28/2008 NXP, B.V.				EXAMINER		
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Please find below and/or attached an Office communication concerning this application or proceeding.

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Application No. Applicant(s) 10/550.853 MEUNIER-BEILLARD ET AL. Office Action Summary Examiner Art Unit KHIEM D. NGUYEN 2823 -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS. WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status 1) Responsive to communication(s) filed on 23 July 2008. 2a) This action is FINAL. 2b) This action is non-final. 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. Disposition of Claims 4) Claim(s) 1-17 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) 8-12 is/are allowed. 6) Claim(s) 1-7 and 13-16 is/are rejected. 7) Claim(s) 17 is/are objected to. 8) Claim(s) _____ are subject to restriction and/or election requirement. Application Papers 9) The specification is objected to by the Examiner. 10) The drawing(s) filed on is/are; a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abevance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152. Priority under 35 U.S.C. § 119 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. Attachment(s)

1) Notice of References Cited (PTO-892)

Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO/SE/08)
Paper No(s)/Mail Date ______

Interview Summary (PTO-413)
 Paper No(s)/Mail Date. ______.

6) Other:

Notice of Informal Patent Application

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DETAILED ACTION

Remarks

1. Applicants' arguments, see (page 6, lines 13-27), filed on July 23rd, 2008, with respect to the rejection(s) of claim(s) 1-3, 5, 13 and 15-16 under 35 U.S.C. 102(b) have been fully considered and are persuasive. Therefore, the non-final rejection as set forth in paper No. 20080415 has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Meyerson (EP 0459 122) and Agnello (Applied Physics Letter 1992, pages 1298-1300). Claims 1-17 are pending in the application.

Claim Rejections - 35 USC § 103

- The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- Claims 1-6 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meyerson (EP 0 459 122) in view of Agnello (Applied Physics Letter 1992), both of records.

In re claim 1, <u>Meyerson</u> discloses a method of manufacturing a semiconductor device with a semiconductor body comprising silicon provided with an n-type doped semiconductor region comprising silicon formed by an epitaxial deposition process, wherein the epitaxial deposition process of the n-type region is performed by positioning the semiconductor body in an epitaxial

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reactor (see col. 1, lines 1-38) and introducing in the reactor gas streams comprising a gaseous compound comprising silicon and a gaseous compound comprising an element from the fifth column of the periodic system of elements (see col. 3, line 8 to col. 4, line 23), while heating the semiconductor body to a growth temperature (Tg) (see col. 3, lines 51-58), characterized in that for the gaseous compound comprising silicon a mixture is chosen of a first gaseous silicon compound (silane) which is free of chlorine and a second gaseous silicon compound (chlorosilanes) comprising chlorine (see col. 9, lines 48-51).

However, <u>Meyerson</u> does not specifically disclose introducing in the reactor a first gas stream comprising a carrier gas and using an inert gas as the carrier gas.

Agnello disclose a method of manufacturing a semiconductor device with a semiconductor body comprising silicon provided with an n-type doped semiconductor region comprising silicon formed by an epitaxial deposition process, wherein the epitaxial deposition process of the n-type region is performed by positioning the semiconductor body in an epitaxial reactor and introducing in the reactor a first gas stream comprising a carrier gas and further gas streams comprising a gaseous compound comprising silicon and a gaseous compound comprising an element from the fifth column of the periodic system of elements while heating the semiconductor body to a growth temperature (Tg) and using an inert gas as the carrier gas (see page 1298, 1st and 2nd paragraphs).

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As <u>Agnello</u> disclosed, one of ordinary skill in the art would have been motivated to introduce in the reactor a first gas stream comprising a carrier gas and using an inert gas as the carrier gas in order to exhibit excellent surface morphology and were virtually free from extended twinning defects as determined by XTEM and PVTEM analysis (see page 1299, 4th paragraph of Agnello).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to modify <u>Meyerson</u> reference with the step of introducing in the reactor a first gas stream comprising a carrier gas and using an inert gas as the carrier gas as taught by <u>Agnello</u> in order to exhibit excellent surface morphology and were virtually free from extended twinning defects as determined by XTEM and PVTEM analysis (see page 1299, 4th paragraph of Agnello).

In re claim 2, as applied to claim 1 above, <u>Meverson</u> in combination with <u>Agnello</u> disclose all claimed limitations including the limitation characterized in that the first gaseous silicon compound silane (SiH₄) is chosen and for the second gaseous silicon compound dichlorosilane (SiH₂Cl₂) is chosen (see col. 9, lines 48-51 of Meyerson).

In re claim 3, as applied to claim 1 above, <u>Meverson</u> in combination with <u>Agnello</u> disclose all claimed limitations including the limitation characterized in that for the gaseous compound comprising a V-element, phosphine is chosen (see col. 4, lines 13-23 of Meverson).

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In re claim 4, as applied to claim 1 above, <u>Meverson</u> in combination with <u>Agnello</u> disclose all claimed limitations including the limitation characterized in that for the growth temperature (Tg) a temperature in the range between 500 °C and 600 °C is chosen (see col. 2, lines 11-21 of Meyerson).

In re claim 5, as applied to claim 1 above, <u>Meverson</u> in combination with <u>Agnello</u> disclose all claimed limitations including the limitation characterized in that the epitaxial deposition process is performed at reduced pressure (P) (see col. 1, lines 1-14 of Meyerson).

In re claim 6, as applied to claim 1 above, <u>Meyerson</u> in combination with <u>Agnello</u> disclose all claimed limitations including the limitation characterized in that a pressure (P) is chosen between 120 and 160 Torr (see col. 7, lines 6-16 of Meyerson).

In re claim 13, as applied to claim 1 above, <u>Meverson</u> in combination with <u>Agnello</u> disclose all claimed limitations including the limitation characterized in that nitrogen is chosen as the inert gas (see page 1298, 2nd paragraph of Agnello).

In re claim 14, as applied to claim 1 above, <u>Meverson</u> in combination with <u>Agnello</u> disclose all claimed limitations including the limitation characterized in that the semiconductor region or the further semiconductor region are formed as a mixed crystal of silicon and germanium by leading yet another gas stream to the reactor comprising a gaseous compound of germanium (see col. 3, lines 8-17 of Meyeson).

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In re claim 15, as applied to claim 1 above, <u>Meyerson</u> in combination with <u>Agnello</u> disclose the semiconductor device obtained by the method as recited in claim 1 (see col. 1, lines 1-14 of Meyerson).

In re claim 16, as applied to claim 1 above, <u>Meverson</u> in combination with <u>Agnello</u> disclose all claimed limitations including the limitation characterized in that the apparatus comprises a deposition reactor and is provided with a first source for a gaseous compound of silicon (silane) (SiH₄) which is free of chlorine and a second source for a gaseous compound of silicon (dichlorosilane) (SiH₂Cl₂) which comprises chlorine (see col. 9, lines 48-51 of Meyerson).

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Meyerson (EP 0 459 122) in view of Agnello (Applied Physics Letter 1992) as applied to claim 1 above, and further in view of Mizushima et al. (U.S. Patent 6,395,621), all of records.

In re claim 7, as applied to claim 1, Paragraph 3 above, <u>Meyerson</u> in combination with <u>Agnello</u> do not specifically disclose characterized in that for the semiconductor device a MOSFET device is chosen and the semiconductor region is formed as a source or drain of the MOSFET device.

Mizushima et al., however, disclose a method of manufacturing a MOSFET device wherein a semiconductor region which is formed by epitaxial growth technique is an elevated source/drain structure of the MOSFET device (see col. 16, lines 6-47 and FIGS. 12A-D).

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As <u>Mizushima et al.</u> disclose, one of ordinary skill in the art would have been motivated to provide an epitaxially grown semiconductor region which is formed as a elevated source or drain structure of the MOSFET device in order to raise the density and the performance of the semiconductor device and furthermore, to reducing the manufacturing steps and lower the cost of the material (see col. 4, lines 14-21 of Mizushima et al.). As known to one of ordinary skill in the art, epitaxially formed elevated source/drain architecture is a possible route for deep submicron CMOS and has been proved effective in allowing both junction depth reduction and leakage control of silicided junctions, thereby resulting in scalability.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to modify Meyerson and Agnello references with the method of epitaxially forming the elevated source/drain structure for the MOSFET device as taught by Mizushima et al. in order to raise the density and the performance of the semiconductor device and furthermore, to reducing the manufacturing steps and lower the cost of the material (see col. 4, lines 14-21 of Mizushima et al.). Additionally, epitaxially formed elevated source/drain architecture is a possible route for deep submicron CMOS and has been proved effective in allowing both junction depth reduction and leakage control of silicided junctions, thereby resulting in scalability.

Allowable Subject Matter

Claims 8-12 are allowed over prior art of record.

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Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons For Allowance

7. After further search and consideration of Applicants' response, it is determined that the prior art of record neither anticipates nor renders obvious the claimed subject matter of the instant application as a whole taken alone or in combination, in particular, prior art of record does not teach "after the growth of the n-type semiconductor region comprising silicon the deposition process is continued with the growth of a further semiconductor region comprising a lower n-type doping than the semiconductor region or comprising a p-type doping and in that at least between the growth of the semiconductor region and the growth of the further semiconductor region, the inert carrier gas is replaced by a carrier gas comprising hydrogen", as recited in claim 8 and "a first carrier gas source comprising an inert gas and a second carrier gas source comprising hydrogen and with means to switch the carrier gas from the inert gas to hydrogen during the deposition process", as recited in claim 17.

Claims 9-12 also allowed to as being directly or indirectly dependent of the allowed base claim.

Response to Applicants' Amendment and Arguments

Applicants' arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection. Art Unit: 2823

Conclusion

9. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to KHIEM D. NGUYEN whose telephone number is

(571)272-1865. The examiner can normally be reached on Monday-Friday (8:30

AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the

examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907.

The fax phone number for the organization where this application or proceeding

is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from

the Patent Application Information Retrieval (PAIR) system. Status information

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9199 (IN USA OR CANADA) or 571-272-1000.

/Khiem D. Nguyen/ Examiner, Art Unit 2823

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